4E2149

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B. Tech. (Sem. IV) (Main/Back) Examination, June/July - 2011
Electrical & Electronics Engg.
4EX2 Digital Electronics

Time : 3 Hours] [Total Marks : 80
[Min. Passing Marks : 24

*Attempt any **five** questions. Selecting **one** question from each unit. All questions are carry **equal** marks.*
(Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used/calculated must be stated clearly

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. Nil 2. Nil

UNIT - I

1 (a) Find the radix of the given number system.

(i) $(23)_x + (12)_8 = (1B)_{16}$

(ii) $(110)_x + (15)_x = (29)_x$

4+4

(b) List the major advantages of digital electronics over analog electronics. 4

(c) What is the advantages of using Gray code ? Explain any one area of its application with the help of a block diagram. 4

OR

1 (a) Realize the following expressions :

(i) $Y = \left(ABC + \overline{BC}\right)C$ using NOR gates only

(ii) $Y = (AB + BC)C$ using NAND gates only

4+4

(b) What is reflective code ? With the help of an example explain the difference between reflective and sequential code. 4

(c) A seven bit hamming code is received as 1101011 is the received code correct ? If not then find the correct code which was transmitted. 4

UNIT - II

2 (a) Why CMOS IC's are preferred for battery operated function? **2**

(b) Explain the role of diode D in the output circuit of totem - pole output gate. What will happen if it is removed from the circuit ? **4**

(c) Compare different parameters of TTL and CMOS logic families. **10**

OR

2 (a) What parameters have to be taken care while driving a CMOS gate by a TTL gate ? **2**

(b) Why ECL family is the fastest logic family ? Explain. **4**

(c) Explain the interfacing concept of TTL gate driving a CMOS gate with equal power supply voltage. **10**

UNIT - III

3 (a) Minimize the following equation using K - map. Realize the output equation using NAND gates only.

$Y = M_0, M_2, M_4, M_6, M_7$

(b) Find the minimal expression using Quine-Mc Cluskey method.

$f(A,B,C,D) = \sum m(1,5,6,12,13,14) + d(2,4)$ **10**

(c) Design a digital circuit which accepts inputs between 0 to 9 and generates logic '1' if the input is an odd number and '0' if the input is even number. **6**

(d) If $W(A,B,C,D) \sum m(0,1,2,3,4,6,7,10,11,12,15)$

$X(A,B,C,D) \sum m(0,1,2,5,6,9,10,11,12,13,14)$

Find $Y = W \oplus X$ and realize the output equation using NAND gates only. **10**

UNIT - IV

4 (a) Explain in easy steps how a full subtractor can be implemented using 4 : 1 multiplexers. **8**

(b) Implement 3 - input OR and Ex OR gate using 2 : 1 multiplexers. **8**

OR

4 (a) With the help of neat circuit diagram explain the experimental setup of BCD to seven segment decoder process using 7447 IC. Explain how leading zero's are eliminated in multi-digit display. **8**

(b) Explain in easy steps how a full adder can be implemented using 1 : 4 demultiplexers. **8**

UNIT - V

5 (a) With the help of an excitation table explain how a D - flip - flop can be converted into T flip - flop. **8**

(b) What is a ring counter ? Where it is used ? If in a 4 - bit ring counter due to false triggering an extra bit is initiated in the ring, say 1001. Explain how this extra bit will be eliminated from the ring counter. **8**

OR

5 (a) With the help of an excitation table, explain how a 3 - bit synchronous up counter can be designed using T - flip - flops. **8**

(b) With the help of simple circuit diagram explain the difference in working of asychronous and synchronous counter. **8**
